COURSE STRUCTURE
AND
DETAILED SYLLABUS
(MR14 Regulations)

For
M.Tech. (EMBEDDED SYSTEMS)
(Applicable for the batches admitted from academic year 2014-15)

Department of Electronics & Communication Engineering
MALLA REDDY ENGINEERING COLLEGE
(Autonomous)
Maisammaguda, Dulapally (post & via Kompally), Secunderabsd-500 100
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MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

Maisammaguda, Dhulapally (Post via. Kompally), Secunderabad - 500100

ACADEMIC REGULATIONS MR 14 FOR M. TECH. (REGULAR) DEGREE COURSE

(Effective for the students admitted into first year from the academic year 2014-2015)

The M.Tech Degree of Malla Reddy Engineering College, Hyderabad shall be conferred on candidates by the Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad who are admitted to the program and fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to the eligibility, qualifications and Specialization as prescribed by the university/college from time to time.

Admissions shall be made on the basis of merit/rank obtained by the qualifying candidate at an Entrance Test conducted by the University/college or on the basis of any other order of merit approved by the University/college (say **PGECET/GATE**) subject to reservations as laid down by the Government from time to time.

2.0 AWARD OF M. TECH. DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after four academic years of course work.

2.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four Academic years from the year of his admission, shall forfeit his seat in M. Tech. course.

2.3 The student shall register for all 88 credits and secure all the 88 credits.

2.4 The minimum instruction days in each semester are 90.

3.0 COURSES OF STUDY

The following specializations are offered at present for the M. Tech. course of study.

1. Advanced Manufacturing Systems(AMS) - Shift II
2. Computer Science(CSE) - Shift I
3. Computer Science and Engineering(CSE) - Shift I & II
4. Control Systems(CS) - Shift I & II
5. Digital Systems and Computer Electronics(DSCE) - Shift I
6. Electrical Power Systems (EPS) - Shift I
7. Embedded Systems(ES) - Shift I
8. Geotechnical Engineering(GTE) - Shift I
9. Machine Designs (MD) - Shift I
10. Power Electronics and Electrical Drives(PEED) - Shift II
11. Structural Engineering(SE) - Shift I
12. Transportation Engineering(TE) - Shift II
13. Thermal Engineering(THE) - Shift I
14. VLSI System Design(VLSI SD) - Shift I

3.1 Departments offering M. Tech. Programmes with specializations are noted below:

Branch	Specialization	Specialization Code
Civil Engineering	1. Structural Engineering (SE) 2. Transportation Engineering (TE) 3. Geotechnical Engineering (GE)	11 12 13
Electrical and Electronics Engineering	1. Control Systems (CS) 2. Power Electronics and Electric Drives (PEED) 3. Electrical Power Systems (EPS)	22 23 24
Mechanical Engineering	1. Thermal Engineering (TE) 2. Advanced Manufacturing Systems (AMS) 3. Machine Designs (MD)	31 32 33
Electronics and Communication Engineering	1.Digital Systems and Computer Electronics (DSCE) 2. VLSI System Design (VLSI SD) 3. Embedded Systems (ES)	41 42 43
Computer Science and Engineering	1. Computer Science and Engineering (CSE) 2. Computer Science (CSE)	51 52

4.0 ATTENDANCE

The programs are offered on a unit basis with each subject being considered as a unit.

4.1 A student shall be eligible to write University examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

4.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

4.3 Shortage of Attendance below 65% in aggregate shall not be condoned.

4.4 Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class and their registration shall stand cancelled.

4.5 A prescribed fee shall be payable towards Condonation of shortage of attendance.

4.6 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

4.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirements of the previous semester including the days of attendance in sports, games, NCC and NSS activities.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the **average** of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each midterm examination shall be conducted for a total duration of 120 minutes with Part A as 2 questions to be answered out of 4 questions each question for 10 marks and Part B with 4 questions to be answered out of 6 questions each question for 5 marks. If any candidate is absent for any subject of a mid -term examination, an additional exam will be conducted in the deserving cases based on the recommendations of the College Academic Committee. End semester examination is conducted for 60 marks with 5 questions to be answered out of 8 questions, each question carries 12 marks.

5.2 For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations and 40 marks shall be awarded based on the day-to-day performance as Internal Marks.

5.3 There shall be two seminar presentations during I year I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is intended to assess the students' understanding of various subjects he has studied during the M. Tech. course of study. The Comprehensive Viva-Voce is evaluated for 100 marks by the Committee. There are no internal marks for the Comprehensive Viva-Voce.

5.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.6 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.5) he has to reappear for the End semester Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and so has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled.

5.7 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher and the second examiner shall be another Laboratory Teacher.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation after taking up a topic approved by the Project Review Committee (PRC).

6.1 A Project Review Committee shall be constituted with Principal as chair person, Head of the Department, Coordinator, Supervisor and two other senior faculty members.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical subjects).

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the Departmental Academic Committee for its approval. Only after obtaining the approval of the Departmental Academic Committee can the student initiate the Project work. Departmental Academic Committee (DAC) Consists of Head of the Department as Chairman, along with two Senior Professors and few subject experts too.

6.4 If a candidate wishes to change his supervisor or topic of the project he can do so with approval of Departmental Committee. However, the Departmental Committee shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of topic as the case may be.

6.5 Candidate shall submit status report (in a bound-form) in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated in the beginning of the second year and the duration of the project is for two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal (through Head of the Department) and shall make an oral presentation/demonstration before the PRC.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/ Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the College. For this, Head of the Department shall submit a panel of 3 examiners to the Chief Controller of Examinations of the College, who are eminent in that field with the help of the concerned guide and Head of the department.

6.9 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis, in the time frame as described by PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

6.10 If the report of the examiner is favorable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate's work as one of the following:

A. Excellent
B. Good
C. Satisfactory
D. Not Satisfactory

The Head of the Department shall coordinate and make arrangements for the conduct of Viva- Voce examination.

If the report of the viva-voce is unsatisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, he will not be eligible for the award of the degree unless he is asked to revise and resubmit by the Board.

7.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	% of marks to be secured
First Class with Distinction	70% and above
First Class	Below 70 but not less than 60%
Second Class	Below 60% but not less than 50%
Pass Class	Below 50% but not less than 40%

The marks in internal evaluation and end examination shall be shown separately in the memorandum of marks.

8.0 WITH-HOLDING OF RESULTS

If the candidate has not paid any dues to the university or if any case of in-discipline is pending against him, the result of the candidate will be withheld and he will not be allowed into the next higher semester. The issue of the degree is liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS

9.1 Discontinued, detained or failed candidates are eligible for admission to two earlier or equivalent subjects at a time as and when offered.
9.2 The candidate who fails in any subject will be given two chances to pass the same subject otherwise, he has to identify an equivalent subject as per MR14 academic regulations.

10.0 GENERAL

10.1 The academic regulations should be read as a whole for purpose of any interpretation.
10.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.
10.3 The College may change or amend the academic regulations and syllabus at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the College.
10.4 Wherever the word he, him or his occur, it will also include she, her and hers.
10.5 Wherever the word 'Subject' occurs in the above regulations, it implies the 'Theory Subject' and 'Practical Subject' or 'Lab'.
10.6 Transfers not allowed among group colleges.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any mark son the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over top the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.

3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shallot be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject tithe academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject

6	Refuses to obey the orders of the Chief Superintendent/Assistant –Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-incharge,or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police cases registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.

9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action toward suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
   (i) A show cause notice shall be issued to the college.
   (ii) Impose a suitable fine on the college.
   (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

M.Tech. EMBEDDED SYSTEMS

COURSE STRUCTURE AND SYLLABUS

I Year - I Semester

Code	Subject	L	T	P	Credits	Internal Evaluation	External Evaluation
441A3	Embedded System Design	3	1	0	3	40	60
44104	Microcontrollers for Embedded System Design	3	1	0	3	40	60
44109	Embedded Real Time Operating Systems	3	1	0	3	40	60
44102	Digital System Design	3	1	0	3	40	60
45116 443A1 44101	ELECTIVE I: Advanced Computer Architecture Embedded Computing VLSI Technology and Design	3	1	0	3	40	60
443B1 441B2 45118	ELECTIVE II: Embedded C Soft Computing Techniques Advanced Operating Systems	3	1	0	3	40	60
44301	Embedded system lab-I	0	0	3	2	40	60
44302	Seminar I	0	0	3	2	50	-
	Total	18	6	6	22	330	420

I Year - II Semester

Code	Subject	L	T	P	Credits	Internal Evaluation	External Evaluation
442A1	Hardware software co-design	3	1	0	3	40	60
441D2	Digital signal processors and architectures	3	1	0	3	40	60
44303	Embedded networking	3	1	0	3	40	60
441C1	CPLD and FPGA architectures and applications	3	1	0	3	40	60
443C1 443C2 45117	ELECTIVE III: Sensors and Actuators Ad Hoc Wireless and Sensor Networks Network Security and Cryptography	3	1	0	3	40	60
443D1 441C2 443D2	ELECTIVE IV: Multimedia and Signal Coding System On Chip Architecture Wireless LANs and PANs	3	1	0	3	40	60
44304	Embedded system lab-II	0	0	3	2	40	60
44305	Seminar II	0	0	3	2	50	-
	Total	18	6	6	22	330	420

II Year - I Semester

Code	Subject	L	T	P	Credits	External Evaluation
44306	Comprehensive Viva	-	-	-	2	100
	Project Seminar	-	-	6	2	-
	Project work	-	-	-	-	-
	Total	-	-	6	4	100

II Year - II Semester

Code	Subject	L	T	P	Credits	External Evaluation
44307	Project work & Seminar	-	-	-	40	Grade
	Grade (A/B/C/D)					A. Excellent B. Good C. Satisfactory D. Unsatisfactory

2014-15 CODE: 441A3

MALLAREDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (ES**)** L T/P/D C
I Year I Semester 3 1/-/- 3

EMBEDDED SYSTEMS DESIGN

Course Objectives:

- To introduce the difference between embedded systems and general purpose systems.
- To optimize hardware designs of custom single-purpose processors.
- To compare different approaches in optimizing general-purpose processors.
- To introduce different peripheral interfaces to embedded systems.
- To understand the design tradeoffs made by different models of embedded systems.
- To apply knowledge gained in software-hardware integration in team-based projects.

UNIT -I:
INTRODUCTION TO EMBEDDED SYSTEMS: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II:
TYPICAL EMBEDDED SYSTEM: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III:
EMBEDDED FIRMWARE: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV:
RTOS BASED EMBEDDED SYSTEM DESIGN: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V:
TASK COMMUNICATION: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:
1. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.

REFERENCE BOOKS:
1. Embedded Systems - Raj Kamal, TMH.
2. Introduction to Embedded Systems - Shibu K.V, McGraw Hill.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

Course Outcomes:

- Able to Understand the basics of an embedded system
- Able to write Program in embedded system
- Able to Design, implement and test an embedded system.
- Able to introduce different peripheral interfaces to embedded systems.
- Able to understand the design tradeoffs made by different models of embedded systems.
- Able to apply knowledge gained in software-hardware integration in team-based projects.

2014-15 CODE: 44104

MALLAREDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (ES**)** L T/P/D C
I Year I Semester 3 1/-/- 3

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Course Outcomes:

- To know about ARM Processor Registers, Instruction pipeline, Interrupts and Architecture
- To learn about Instructions, Addressing modes and conditional instructions.
- To learn about Cache architecture, Polices, Flushing, MMU, page tables, translations, and access permissions.

UNIT –I:
ARM ARCHITECTURE: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:
ARM PROGRAMMING MODEL – I: Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:
ARM PROGRAMMING MODEL – II: Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:
ARM PROGRAMMING: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:
MEMORY MANAGEMENT: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:
1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:
1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes /Cole, 1999, Thomas Learning.

Course Outcomes:

- Able to know about ARM Processor Registers, Instruction pipeline, Interrupts and Architecture
- Able to learn about Instructions, Addressing modes and conditional instructions.
- Able to learn about Cache architecture, Polices, Flushing, MMU, page tables, translational, and access permissions.

2014-15 CODE: 44109

MALLAREDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (ES**)** L T/P/D C
I Year I Semester 3 1/-/- 3

EMBEDDED REAL TIME OPERATING SYSTEMS

Course Objectives:

- To emphasize on the concept of a complete system consisting of asynchronous interactions between concurrently executing hardware components and device driver software in order to illustrate the behavior of a computer system as a whole.
- To understand and design RT Linux and Embedded Linux

UNIT – I:
INTRODUCTION: Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II:
REAL TIME OPERATING SYSTEMS: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:
OBJECTS, SERVICES AND I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:
EXCEPTIONS, INTERRUPTS AND TIMERS: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V:
CASE STUDIES OF RTOS: RT Linux, Micro C/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:
1.Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

Course Outcomes:

- Understand the advanced concepts of computer architecture. Exposing the major differentials of RISC and CISC architectural characteristics.
- Able to investigate modern design structures of Pipelined and Multiprocessors systems
- Able to become acquainted with recent computer architectures and I/O devices, as well as the low-level language required to drive/manage these types of advanced hardware.

2014-15 CODE: 44102

MALLAREDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (ES**)** L T/P/D C
I Year I Semester 3 1/-/- 3

DIGITAL SYSTEM DESIGN

Course Objectives:

- To understand about the finite state model, capabilities and limitations of FSM and fundamental mode model.
- To understand how to design the digital circuits using ROM's, PLA's and PAL's.
- To understand about the SM charts and their realization and to implement a binary multiplier and a dice game controller.
- To understand about Fault Modeling & Test Pattern Generation and to learn different algorithms for fault diagnosis of Combinational circuits.
- To understand about different methods for fault diagnosis of Sequential circuits.

UNIT -I:
MINIMIZATION AND TRANSFORMATION OF SEQUENTIAL MACHINES: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cyclesand Hazards.

UNIT -II:
DIGITAL DESIGN: Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner,Binary divider.

UNIT -III:
SM CHARTS: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:
FAULT MODELING & TEST PATTERN GENERATION: Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model. Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:
FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:
1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A.Breuer and Arthur D. Friedman-John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:
1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee, PHI

Course Outcomes:

- The students will have the knowledge about the finite state model, capabilities and limitations of FSM and fundamental mode model.
- The students will how to design the digital circuits using ROM's, PLA's and PAL's.
- The students will have the knowledge of SM charts and their realization and to implement a binary multiplier and a dice game controller.
- The students will have the knowledge of Fault Modeling & Test Pattern Generation and different algorithms for fault diagnosis of Combinational circuits.
- The students will understand about different methods for fault diagnosis of Sequential circuits.

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M. Tech (ES**)** L T/P/D C
I Year I Semester 3 1/-/- 3

ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE -I)

Course Objectives:

- To emphasize on the concept of a complete system consisting of asynchronous interactions between concurrently executing hardware components and device driver software in order to illustrate the behavior of a computer system as a whole.
- To understand the advanced concepts of computer architecture and exposing the major differentials of RISC and CISC architectural characteristics.

UNIT -I:
FUNDAMENTALS OF COMPUTER DESIGN: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

UNIT –II:
PIPELINES: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic fivestage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III:
INSTRUCTION LEVEL PARALLELISM(ILP)-THE HARDWARE APPROACH: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.
ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelismat compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV:
MULTI PROCESSORS AND THREAD LEVEL PARALLELISM: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V:
INTER CONNECTION AND NETWORKS: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:
1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:
1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

Course Outcomes:

- Able to understand the advanced concepts of computer architecture and exposing the major differentials of RISC and CISC architectural characteristics.
- Able to investigating modern design structures of Pipelined and Multiprocessors systems.
- Able to become acquainted with recent computer architectures and I/O devices, as well as the low-level language required to drive/manage these types of advanced hardware.

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EMBEDDED COMPUTING
(ELECTIVE – I)

Course Objectives:

- To learn about System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System and Busy Box
- To know about Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls and network security.
- To learn about IA32 Instruction Set, application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools

UNIT –I:
PROGRAMMING ON LINUX PLATFORM: System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box.
Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT –II:
INTRODUCTION TO SOFTWARE DEVELOPMENT TOOLS:GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools,.

UNIT –III:
INTERFACING MODULES: Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, Open CV for machine vision, Audio signal processing.

UNIT –IV:
NETWORKING BASICS: Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT –V:
IA32 INSTRUCTION SET: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:
1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS:
1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

Course Outcomes:

- Able to learn about System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System and Busy Box
- Able to know about Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls and network security.
- Able to learn about IA32 Instruction Set, application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools

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VLSI TECHNOLOGY AND DESIGN
(ELECTIVE -I)

Course Objectives:

- To Understand the vlsi technology and design of circuits based on technology like cmos bicmos etc
- To Understand the designing layouts of logic gates
- To understanding the combinational logic networks and its optimization
- To understanding the sequential systems and its optimization
- To get knowledge on floor plan design

UNIT –I:
REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:
LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates &Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:
COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:
SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V:
FLOOR PLANNING: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:
1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC

Course Outcomes:
- Student will be in a position that he/she can design vlsi circuits starting from pmos nmos, cmos, and bicmos technology based design
- Gains thorough knowledge on design tools to draw layouts for the transistor structures
- The student will understand the design of logic gates
- The student will understand the design of sequential systems

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EMBEDDED C
(ELECTIVE-II)

Course Objectives:

- Understand the significance of programming embedded C in real time applications and to use it for specific applications.
- To gain knowledge on 8051 micro controller
- To develop code for real time embedded world
- To understand design of real time timers with various constraints
- To understand and gain knowledge on Intruder Alarm System.

UNIT – I:

PROGRAMMING EMBEDDED SYSTEMS IN C : Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

INTRODUCING THE 8051 MICROCONTROLLER FAMILY: Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements , Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT – II:

READING SWITCHES: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs(basic code), Example: Counting goats, Conclusions

UNIT – III:

ADDING STRUCTURE TO THE CODE: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV:

MEETING REAL-TIME CONSTRAINTS: Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V:

CASE STUDY: INTRUDER ALARM SYSTEM: Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008

REFERENCE BOOKS:

1. PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C - Nigel Gardner

Course Outcomes:

- Able to understand the importance embedded C in so many applications like application specific micro controllers
- Able to develop the quality based embedded systems like Intruder Alarm System
- Able to understand the basic working modes of timers and its formatted data frames, its control.

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SOFT COMPUTING TECHNIQUES
(ELECTIVE -II)

Course Objectives:

- To learn about the Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.
- To know about Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm.
- To learn about Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification.

UNIT –I:
INTRODUCTION: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II:
ARTIFICIAL NEURAL NETWORKS: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuronmodel, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III:
FUZZY LOGIC SYSTEM: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self organizingfuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV:
GENETIC ALGORITHM: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and Ant-colony search techniques for solving optimization problems.

UNIT –V:
APPLICATIONS: GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:
1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999.
2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS:
1. Fuzzy Sets, Uncertainty and Information - Klir G.J. &Folger T.A., Prentice-Hall of India Pvt.Ltd. 1993.
2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.
3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.
4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
5. Elements of Artificial Neural Networks - KishanMehrotra, Chelkuri K. Mohan,Sanjay Ranka, Penram International.
6. Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education.
7. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N.Deepa,1/e, TMH, New Delhi.

Course Outcomes:

- Able to learn about the Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system,Rule-based systems, the AI approach, Knowledge representation - Expert systems.
- Able to know about Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm.
- Able to learn about Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning,Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification.

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ADVANCED OPERATING SYSTEMS
(ELECTIVE -II)

Course Objectives:

- To learn about Overview of computer system hardware, Instruction execution, I/O function, Interrupts Memory hierarchy, I/O Communication techniques, Operating system objectives and functions.
- To learn about System calls and related file structures, Input / Output, Process creation & termination.
- To learn about Goals of distributed system, Hardware and software concepts and design issues.

UNIT –I:
INTRODUCTION TO OPERATING SYSTEMS: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II:
INTRODUCTION TO UNIX AND LINUX: Basic commands & command arguments, Standard input, output, Input / output redirection, filter sand editors, Shells and operations

UNIT –III:
SYSTEM CALLS: System calls and related file structures, Input / Output, Process creation & termination.
Inter process communication: Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams &Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:
INTRODUCTION TO DISTRIBUTED SYSTEMS: Goals of distributed system, Hardware and software concepts, Design issues.
Communication in distributed systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:
SYNCHRONIZATION IN DISTRIBUTED SYSTEMS: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions
Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:
1. The design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS:
1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed.John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

Course Outcomes:

- Able to learn about Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions.
- Able to learn about System calls and related file structures, Input / Output, Process creation & termination.
- Able to learn about Goals of distributed system, Hardware and software concepts and design issues.

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EMBEDDED SYSTEMS LAB-I

NOTE:
Minimum of 10 experiments have to be conducted.
The following programs have to be tested on 89C51 Development board/equivalent using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 mS delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions
11. Program to Sort RTOS on to 89C51 development board.
12. Program to interface Elevator.

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HARDWARE SOFTWARE CO-DESIGN

Course Objectives:

- To design mixed hardware-software systems and the design of hardware-software interfaces
- To focus on common underlying modeling concepts, and the trade-offs between hardware and software components.
- To learn about System –level specification, design representation for system level synthesis, system level specification languages.

UNIT –I:
CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co- synthesis algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co synthesis.

UNIT –II:
PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure
Target architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:
COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:
DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:
LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages,
Languages for system – level specification and design-ii: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:
1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010Springer

Course Outcomes:

- Able to design mixed hardware-software systems and the design of hardware-software interfaces
- Able to focus on common underlying modeling concepts, , and the trade-offs between hardware and software components.
- Able to learn about System –level specification, design representation for system level synthesis, system level specification languages.

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DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

Course Objectives:

- Gives an over view of entire digital signal processing techniques i.e. convolution, DFT, FFT, IIR & FIR filters. The fixed and floating point representation, different types of errors introduced during A-D and D-A converter stage
- To introduce the DSP computational building blocks and special types of addressing modes compared to normal microprocessor
- To introduce architectural features of programmable DSP Processors of TMS320C54XX processor. To develop the programming knowledge using Instruction set of DSP Processors
- To introduce architectural features of analog devices family of DSP devices i.e. ADSP 2100, ADSP 2181 and blackfin processor

UNIT –I:
INTRODUCTION TO DIGITAL SIGNAL PROCESSING: Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.
Computational accuracy in dsp implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XXProcessors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:
ANALOG DEVICES FAMILY OF DSP DEVICES: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals

UNIT –V:
INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:
1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach to Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran,
, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M.Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:
1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani andM. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes ,ISBN 0750679123, 2005

Course Outcomes:

- Able to gives an over view of entire digital signal processing techniques i.e. convolution, DFT, FFT, IIR & FIR filters. The fixed and floating point representation, different types of errors introduced during A-D and D-A converter stage
- Able to introduce the DSP computational building blocks and special types of addressing modes compared to normal microprocessor
- Able to introduce architectural features of programmable DSP Processors of TMS320C54XX processor. To develop the programming knowledge using Instruction set of DSP Processors
- Able to introduce architectural features of analog devices family of DSP devices i.e. ADSP 2100, ADSP 2181 and blackfin processor.

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EMBEDDED NETWORKING

Course Objectives:

- To understand the significance of embedded networks in real time applications and to use it for specific applications.
- To Know different types of communication protocols like serial and parallel communication protocols
- To know different types of communication protocols which have embedded end modules
- To understand wired and wireless communication protocols, its formats
- To understand and gain knowledge on wireless sensors and its application in wireless embedded networks

UNIT –I:
Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols –Firewire.

UNIT –II:
USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing –PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III:
Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV:
Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V:
Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing –Data Centric routing.

TEXT BOOKS:
1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, TonyGivargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port -Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:
1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series -Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors – Bhaskar Krishnamachari, Cambridge press 2005.

Course Outcomes:

- Able to understand the basic working modes of networks and its formatted data frames, its control
- Able to understand the significance of embedded networks in real time applications and to use it for specific applications.

- Able to Know different types of communication protocols like serial and parallel communication protocols
- Able to know different types of communication protocols which have embedded end modules
- Able to understand wired and wireless communication protocols, its formats
- Able to understand and gain knowledge on wireless sensors and its application in wireless embedded networks

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CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

Course Objectives:

- To understand the types of programmable logic devices and what are the differences between these devices. What are the different complex programmable logic devices with examples.
- To know the types of FPGA's and their programming technologies. What are the programmable logic block architectures, their interconnects and what are applications of FPGA's.
- To understand about the SRAM programmable FPGA's and their programming technology. What are examples of SRAM programmable FPGA's i.e Xilinx FPGA's with block diagrams.

UNIT-I:
INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II:
FIELD PROGRAMMABLE GATE ARRAYS: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:
SRAM PROGRAMMABLE FPGAS: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 andXC4000 Architectures.

UNIT -IV:
ANTI-FUSE PROGRAMMED FPGAS: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3Architectures.

UNIT -V:
DESIGN APPLICATIONS: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:
1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:
1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design -Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

Course Outcomes:

- The students will have the knowledge of types of programmable logic devices and what are the differences between these devices.
- The students will have the knowledge of types of FPGA's and their programming technologies, programmable logic block architectures, their interconnects and what are applications of FPGA's.
- The students will be able to know the programming technology of SRAM programmable FPGA's with their internal logic diagrams.

MALLAREDDY ENGINEERING COLLEGE
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M. Tech (ES**)** L T/P/D C
I Year II Semester 3 1/-/- 3

SENSORS AND ACTUATORS
(ELECTIVE –III)

Course Objectives:

- To learn about sensor Principles, Classification, Parameters, Characteristics, Environmental Parameters (EP), and Characterization.
- To know about different sensors like Thermal sensors, Magnetic sensors.
- To know about Smart Sensors, Introduction, Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface and the Automation

UNIT -I:
SENSORS / TRANSDUCERS: Principles – Classification – Parameters – Characteristics – Environmental Parameters (EP) – Characterization.
Mechanical and electromechanical sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types- Capacitive Sensors: – Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors

UNIT –II:
THERMAL SENSORS: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermo sensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermo emf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors
Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors –Anisotropic Magneto resistive Sensing – Semiconductor Magneto resistors– Hall Effect and Sensors –Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros –Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flow meter – Switching Magnetic Sensors SQUID Sensors

UNIT -III:
RADIATION SENSORS: Introduction – Basic Characteristics – Types of Photo sensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors. **Electro analytical Sensors:** Introduction – The Electrochemical Cell – The Cell Potential – Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

UNIT -IV:
SMART SENSORS: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation
Sensors –applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring

UNIT -V:
ACTUATORS: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches
Solenoids – D.C. Motors – A.C. motors – Stepper motors

TEXT BOOKS:

1. D. Patranabis – "Sensors and Transducers" –PHI Learning Private Limited.
2. W. Bolton – "Mechatronics" –Pearson Education Limited.

REFERENCE BOOKS:

1. Sensors and Actuators – D. Patranabis – 2nd Ed., PHI, 2013.

Course Outcomes:

- Able to learn about sensor Principles, Classification, Parameters, Characteristics, Environmental Parameters (EP), and Characterization.
- Able to know about different sensors like Thermal sensors, Magnetic sensors.
- Able to know about Smart Sensors, Introduction, Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface and the Automation

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AD HOC WIRELESS AND SENSOR NETWORKS
(ELECTIVE-III)

Course Objectives:

- To learn about Introduction, Fundamentals of WLANS, IEEE802.11 Standard, HIPERLAN Standard, Bluetooth and Home RF.
- To learn about Issues in Ad Hoc Wireless Networks, AD Hoc Wireless Internet.MAC Protocols for Ad Hoc Wireless Networks and Issues in designing a MAC protocol for Ad Hoc Wireless network.
- To learn about issues in designing a routing protocol for ad hoc wireless networks, classification of routing protocols, tabel-driven routing protocols on-demand routing protocols, hybrid routing protocols, routing protocols with efficient flooding mechanism, hierarchical; routing protocols, power-aware routing protocols.

UNIT-I

WIRELESS LANS AND PANS: Introduction, Fundamentals of WLANS, IEEE802.11 Standard. HIPERLAN Standard, bluetooth, Home RF. Wireless Internet: Wireless internet, mobile IP, TCP in Wireless Domain, WAP, Optimizing Web over Wireless.

UNIT-II

Adhoc wireless networks: Introduction, Issues in Ad Hoc Wireless Networks, AD Hoc Wireless Internet.MAC Protocols for Ad Hoc Wireless Networks: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless network, Design goals of MAC Protocol, contention - Based Protocols, contention -based protocol with Reservation Mechanism, contention - Based MAC Protocols with Scheduling Mechanisms, MAC protocol that use Directional Antenna, other MAC Protocol

UNIT-III

ROUTING PROTOCOLS: introduction issues in designing a routing protocol for ad hoc wireless networks, classification of routing protocols, table-driven routing protocols, on-demand routing protocols, hybrid routing protocols, routing protocols with efficient flooding mechanism, hierarchical; routing protocols, power-aware routing protocols.

Transport layer and security protocols: introduction, issues in designing a transport layer protocol for ad hoc wireless networks, design goals of a transport layer protocol for ad hoc wireless networks, classification of transport layer solutions, TCP over ad hoc wireless networks, other transport layer protocol fpr ad hoc wireless networks, security provisioning, network security attacks, key management, secure routing in ad hoc wireless networks

UNIT-IV:

QUALITY OF SERVICE: Introduction, issuses and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions, MAC Layer solutions, Network layer solutions, QoS Frame Works for Ad Hoc Wireless Network**. Energy management**: Introduction, Need for Energy Management in Ad Hoc Wireless Networks, Classification of Ad Hoc Wireless networks, Battery Management Schemes, Transmission Power Management Schemes, System power management schemes.

UNIT-V:

WIRELESS SENSOR NETWORKS: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocol for Sensor Networks, Location Discovery, Quality of Sensor Networks, Evolving Standards, Other Issues.

TEXT BOOKS:

1. Ad HOC Wireless Networks: Architectures and protocols-C.Siva Ram Murthy and B.S.Manoj, 2004,PHI
2. Wireless Ad-Hoc and Sensor Networks: Protocols,Performance and control –Jagannatham Sarangapani,CRC Press

REFERENCE BOOKS:

1. Ad -Hoc Mobile Wireless Networks:Protocols And Systems,C.K.Toh,1ed.Pearson Education.
2. Wireless Sensor Networks -C.S. Raghavendra, Krishna m.Sivalingam,2004,Springer

Course Outcomes:

- Able to learn about Introduction, Fundamentals of WLANS, IEEE802.11 Standard, HIPERLAN Standard, Bluetooth and Home RF.
- Able to learn about Issues in Ad Hoc Wireless Networks, AD Hoc Wireless Internet.MAC Protocols for Ad Hoc Wireless Networks and Issues in designing a MAC protocol for Ad Hoc Wireless network.
- Able to learn about issues in designing a routing protocol for ad hoc wireless networks, classification of routing protocols, tabel-driven routing protocols, on-demand routing protocols, hybrid routing protocols, routing protocols with efficient flooding mechanism, hierarchical; routing protocols, power-aware routing protocols.

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M. Tech (ES**)** L T/P/D C
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NETWORK SECURITY AND CRYPTOGRAPHY
(ELECTIVE– III)

Course Objectives:

- To know about Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security
- To know about Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
- To know about IP Security Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management

UNIT –I:
INTRODUCTION: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT –II:
MODERN TECHNIQUES: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2,
Characteristics of Advanced Symmetric block cifers. **Conventional encryption:** Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation. **Public key cryptography:** Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT –III:
NUMBER THEORY: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler'stheorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.
Message authentication and hash functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT –IV:
HASH AND MAC ALGORITHMS: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. **Digital signatures and authentication protocols**: Digital signatures, Authentication Protocols, Digital signature standards. **Authentication applications**: Kerberos, X.509 directory Authentication service. Electronic Mail
Security: Pretty Good Privacy, S/MIME.

UNIT –V:
IP SECURITY: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.
Web security: Web Security requirements, Secure sockets layer and Transport layer security,Secure Electronic Transaction.
Intruders, viruses and worms: Intruders, Viruses and Related threats.
Fire walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:
1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.

REFERENCE BOOKS:
1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
2. Network Security - Private Communication in a Public World by Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.
3. Principles of Information Security, Whitman, Thomson.

4. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH
5. Introduction to Cryptography, Buchmann, Springer.

Course Outcomes:

- Able to know about Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security
- Able to know about Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
- Able to know about IP Security Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management

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I Year II Semester 3 1/-/- 3

MULTI MEDIA AND SIGNAL CODING
(ELECTIVE -IV)

Course Objectives:

- To learn about Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.
- To know about Lossless compression algorithms like Run Length Coding, Variable Length Coding, Arithmetic Coding and Lossless JPEG image Compression.
- To learn about Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT -I:
INTRODUCTION TO MULTIMEDIA: Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.
COLOR IN IMAGE AND VIDEO: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Out of-Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

UNIT -II:
VIDEO CONCEPTS: Types of Video Signals, Analog Video, Digital Video.
AUDIO CONCEPTS: Digitization of Sound, Quantization and Transmission of Audio.

UNIT -III:
COMPRESSION ALGORITHMS: Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression. **Lossy Image Compression Algorithms:** Transform Coding: KLT And DCT Coding, Wavelet Based Coding. **Image Compression Standards:** JPEG and JPEG2000.

UNIT -IV:
VIDEO COMPRESSION TECHNIQUES: Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding,Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT -V:
AUDIO COMPRESSION TECHNIQUES: ADPCM in Speech Coding, G.726 ADPCM, Vocoders – Phase Insensitivity, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

TEXT BOOKS:
1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.
2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition, 2009

REFERENCE BOOKS:
1. Multimedia Communication Systems – Techniques, Stds &Netwroks K.R. Rao, Zorans.Bojkoric, DragoradA.Milovanovic, 1st Edition, 2002.
2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition,2009.
3. Multimedia Systems John F. KoegelBufond Pearson Education (LPE), 1st Edition, 2003.
4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.

5. Video Processing and Communications – Yaowang, JornOstermann, Ya-QinZhang, Pearson,2002

Course Outcomes:

- Able to learn about Multimedia, World Wide Web, Overview of Multimedia Tools,Multimedia Authoring, Graphics/ Image Data Types, and File Formats.
- Able to know about Lossless compression algorithms like Run Length Coding, Variable Length Coding, Arithmetic Coding and Lossless JPEG image Compression.
- Able to learn about Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

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M. Tech (ES**)** L T/P/D C
I Year II Semester 3 1/-/- 3

SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -IV)

Course Objectives:

- Instruction to system approach deals with how system assembled with the components, which components are involved in the system integration.
- To introduce hardware and software programmability verses performance
- To know about entire memory organization, starch pads, cache memories and objective in cache data how to deal the write polices

UNIT –I:
INTRODUCTION TO THE SYSTEM APPROACH: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II:
PROCESSORS: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:
MEMORY DESIGN FOR SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV:
INTERCONNECT CUSTOMIZATION AND CONFIGURATION: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:
APPLICATION STUDIES / CASE STUDIES: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:
1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely IndiaPvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:
1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, PeterPaterson and Leena Singh L, 2001, Kluwer Academic Publishers.

Course Outcomes:

- Able to about how the system forms with the lot of component and has majority about system level interconnections
- Able to introduce hardware and software programmability verses performance
- Able to know about entire memory organization, starch pads, cache memories and objective in cache data how to deal the write polices

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MALLAREDDY ENGINEERING COLLEGE
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M. Tech (ES**)** L T/P/D C
I Year II Semester 3 1/-/- 3

WIRELESS LANS AND PANS
(ELECTIVE-IV)

Course Objectives:

- To learn about First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems.
- To know about importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies infrared technology, UHF narrowband technology, Spread Spectrum technology
- To learn about Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem and Reliability.

UNIT –I:
WIRELESS SYSTEM & RANDOM ACCESS PROTOCOLS: Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).

UNIT –II:
WIRELESS LANS: Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology

UNIT –III:
THE IEEE 802.11 STANDARD FOR WIRELESS LANS: Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol

UNIT –IV:
WIRELESS PANS: Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications,
technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scatter net formation.

UNIT –V:
THE IEEE 802.15 WORKING GROUP FOR WPANS: The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.

TEXT BOOKS:
1. Ad Hoc and Sensor Networks - Carlos de Morais Cordeiro and Dharma Prakash Agrawal,World Scientific, 2011.
2. Wireless Communications and Networking - Vijay K.Garg, Morgan Kaufmann Publishers, 2009.

REFERENCE BOOKS:
1. Wireless Networks - KavehPahlaram, Prashant Krishnamurthy, PHI, 2002.
2. Wireless Communication- Marks Ciampor, Jeorge Olenewa, Cengage Learning, 2007.

Course Outcomes:

- Able to learn about First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems.
- Able to know about importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies infrared technology, UHF narrowband technology, Spread Spectrum technology
- Able to learn about Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem and Reliability.

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M. Tech (ES**)** L T/P/D C
I Year II Semester - -/3/- 2

EMBEDDED SYSTEM LAB – II

A. The following programs are to be implemented on ARM based Processors/Equivalent.

B. Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

PART- I:

The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for

a. Addition | Subtraction | Multiplication | Division b. Operating Modes, System Calls and Interrupts c. Loops, Branches

2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.

3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.

4. Program for reading and writing of a file

5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment

6. Program to demonstrates a simple interrupt handler and setting up a timer

7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.

8. Program to Interface 8 Bit LED and Switch Interface

9. Program to implement Buzzer Interface on IDE environment

10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.

11. Program to demonstrate I2C Interface on IDE environment

12. Program to demonstrate I2C Interface – Serial EEPROM

13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.

14. Generation of PWM Signal

15. Program to demonstrate SD-MMC Card Interface.

PART- II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.

2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task

3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher

priority than external interrupt button)

4. a).Write an application to Test message queues and memory blocks.
   b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment